Design and Analysis of a 4.2 mW 4 K 6–8 GHz CMOS LNA for Superconducting Qubit Readout

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***Abstract*— This article proposes a cryogenic inverter-based low noise amplifier (LNA) for qubit readout. Its input impedance matching is realized by a high-Q ON-chip gate inductor and capacitive load through the gate-to-drain feedback capacitance of the input transistors. Cascode transistors are used to optimize the impedance matching, which results in a larger gate inductor and smaller load capacitor and hence a higher passive and inverter gain. Owing to the high passive gain and Q-factor of the gate inductor at 4 K, the noise of the active stages is substantially suppressed with a negligible noise contribution of the gate inductor. Moreover, with the current re-use in the inverter topology, less power consumption is achieved for the given transconductance of transistors. The input impedance, gain, and noise analyses of the proposed LNA are performed for room temperature (RT) operation, and its noise optimization is done by taking the cryogenic operation of the devices into account. We demonstrate with the circuit analysis and measurement results that the input impedance of the LNA has a low sensitivity to variations on device parameters at cryogenic temperatures. The LNA is implemented in a 28 nm CMOS technology. It achieves 0.4–0.7 dB noise figure (NF) with 4.2 mW power consumption at 4 K, and its operating frequency is between 6–8 GHz. The LNA consumes very low power compared to the state-of-the-art cryogenic CMOS LNAs while providing similar NF performance at 4 K, which makes it suitable for dilution refrigerators.**

***Index Terms*— Capacitive feedback, cascode, cryogenic CMOS, high-Q ON-chip inductor, inverter-based low-noise amplifier (LNA), low power, quantum computing.**

I. Introduction

THE immense potential of quantum computing for solving intricate problems in various fields such as chemistry and biology encourages many institutions and leading technology companies to do research on quantum computers (QCs). With this motivation and extensive development, quantum supremacy has been already demonstrated with 53 qubits [1], and QCs are expected to break the 1000-qubit barrier in the coming years. At that stage, the employment of numerous cables and bulky circulators used to connect room temperature (RT) control and readout circuitries to qubits in dilution refrigerators is anticipated to be a bottleneck in scaling QCs. Cryo-CMOS circuitries are a promising solution to tackle this problem by accommodating control and readout circuitries at the 1–4 K stages of dilution refrigerators being physically closer to qubits [2]. Moreover, they can be co-integrated with spin qubits to reduce the system complexity as demonstrated in [3]. One of the greatest challenges for this approach is the power dissipation constraint (a few Watts) at the 4 K stage of the dilution refrigerators.

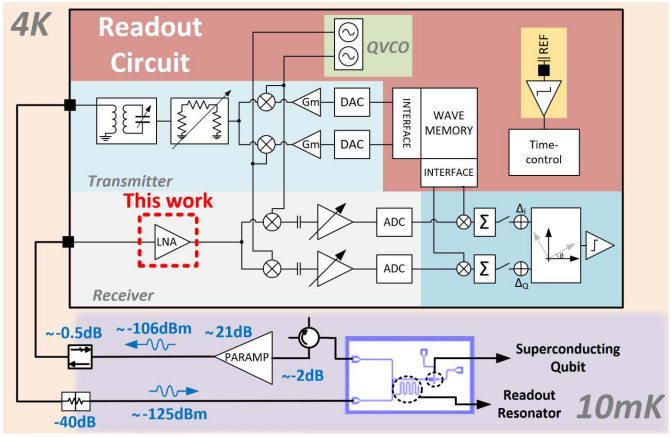

Fig. 1. Dispersive qubit measurement diagram using the cryo-CMOS readout circuitry at 4 K, where the designed LNA is integrated [7].

The dispersive readout of the superconducting qubits is illustrated in Fig. 1. To determine the state of a superconducting qubit, a very weak single tone (e.g., −125 dBm) is transmitted to the readout resonator of the qubit, and there it is modulated through the admittance of the qubit determined by its state [4]. Aiming to detect this weak modulated signal obliges to use parametric amplifiers at base temperature whose noise temperature can ideally go down to 0.144 K at 6 GHz with very minimal power consumption [5]. However, parametric amplifiers do not reach the required linearity level to attain sufficient amplification of the quantum information signal before further processing. Therefore, the additional signal amplification is usually done by cryogenic HEMTs since they can achieve a noise temperature of a few Kelvins with <1 mW power consumption [6].

Receivers fully implemented in CMOS technologies have recently become a focus of research to achieve a more compact and cost-efficient readout system where cryogenic CMOS

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low noise amplifiers (LNAs) play a crucial role. In [2], the cryo-LNA designed in a 0.16 μm CMOS process demonstrates that compared to HEMTs, cryo-CMOS LNAs can achieve a competitive noise performance with ∼0.1 dB noise figure (NF) at the operating frequency of 0.1–0.5 GHz, but at a power consumption of 54.9 mW. Also, in the higher frequency range, the best NF reported among cryo-CMOS LNAs is between 0.23–0.65 dB with 39 mW power consumption in the frequency range of 4.6–8.2 GHz implemented in 40 nm CMOS technology [8]. This is mainly ascribed to the shot noise which does not depend on the ambient temperature [8], [9], [10]. To reduce the shot noise, the channel length of transistors should be long, and transistors should operate with a high V_{gs} [11]. This necessitates a high-power dissipation for cryo-CMOS LNAs, which is undesired in quantum computing applications due to the limited cooling power of the dilution refrigerators, and it can give rise to a substantial self-heating at 4 K resulting in a higher thermal noise [12]. At higher operating frequencies, considering that transistors with a shorter channel length are used to have a sufficiently high f_T, the shot noise becomes more critical in this case for cryogenic NF performance.

The source degenerated cascode LNA topology is extensively used in cryogenic applications; however, they consume a significant power while they achieve the NF of 0.4–0.6 dB at 4 K in the frequency range of 6–8 GHz [8], [13], [14]. In this article, we propose a power-efficient solution for cryo-CMOS LNAs to achieve a decent NF at cryogenic temperatures and to be compliant with the power dissipation constraint of dilution refrigerators at the same time [15]. The proposed LNA is integrated into a readout circuitry designed for a single superconducting qubit readout operation between 6–8 GHz as shown in Fig. 1. We use a cascoded inverter topology with a large high-Q ON-chip gate inductor which provides a high passive gain thereby significantly suppressing the channel noise of transistors without burning additional power. With this LNA topology, we accomplish a similar NF performance at 4 K as its previously published CMOS counterparts, however, with an order of magnitude lower power consumption.

The organization of this article is as follows. The LNA performance requirements for superconducting qubit readout applications are described in Section II. The input impedance, gain, and noise of the LNA are analyzed in Section III. The device performances at cryogenic temperatures are discussed, and the design procedure of the LNA is illustrated in Section IV. The measurement and simulation results are provided in Section V. The conclusion is drawn in Section VI.

II. LNA Specifications for Superconducting Qubit Readout

As elaborated in [4], for a typical superconducting qubit readout operation, the receiver noise temperature (T_{RX}) has to be roughly 0.56 K to reach a 1% readout error rate at 5 GHz measurement frequency, which corresponds to approximately 0.67 K at 6 GHz. Cryogenic parametric amplifiers have to be used in the first stage of the readout receiver chain to achieve this ultra-low noise performance as illustrated in Fig. 1 [4]. Their noise temperature can be as low as the standard quantum limit (SQL) (≈24 mK/GHz), and with circulator and cable losses (∼2 dB) before parametric amplifiers, its total noise temperature practically reaches two times the SQL [5]. Therefore, the parametric amplifier noise temperature (T_{Pamp}) can be assumed as 0.288 K at 6 GHz. Given that the 1-dB compression point of the parametric amplifiers can go up to −100 dBm [16], and the readout resonator drive power is typically −125 dBm, the received signal can first be amplified by 21 dB gain (G_{Pamp}) using a parametric amplifier at 10 mK [17].

TABLE I
LNA Target Specifications at 4 K for Superconducting Qubit Readout

Conditions		Target Specifications			
Freq.	**BW**	**NF**	**Gain**	**Power**	**IP1dB**
6 GHz	2 GHz	<0.6 dB	>40 dB	<10 mW	> −105 dBm

Supposing that the LNA has sufficiently high gain to overcome the noise at the rest of the receiver chain, the receiver noise temperature in Fig. 1 can be expressed as

$$T_{RX} = T_{Pamp} + \frac{(L-1)\cdot T_{Phys}}{G_{Pamp}} + \frac{T_{LNA}\cdot L}{G_{Pamp}} \quad (1)$$

where T_{Phys} is the physical temperature of the isolator. The insertion loss of an isolator with >40 dB isolation is ∼0.2 dB [18]. Together with the cable loss, we can assume that the total insertion loss (L) between the parametric amplifier and the LNA is roughly ∼0.5 dB. In this case, the maximum noise temperature value of the LNA (T_{LNA}) has to be 43 K (0.6 dB NF) at 6 GHz to accomplish $T_{RX} = 0.67$ K according to (1).

In addition, the total power dissipation at the 4 K stage should be less than 1 mW/qubit for a 1000-qubit system [2]. Given that the full cryo-CMOS system for qubit readout and control will also be accommodated at the 4 K stage, the LNA power consumption limit can be set to 0.1 mW/qubit. Frequency-division multiplexing (FDM) technique is widely used to meet these ultralow power requirements [13], [14]. Owing to the high-quality factor of readout resonators [19], FDM can be implemented in the readout with 10 MHz resonator bandwidth and 10 MHz spacing for each qubit. Therefore, a 6–8 GHz LNA can perform a simultaneous readout of 100 qubits. In this case, the maximum LNA power consumption must be 10 mW to achieve 0.1 mW/qubit.

Thanks to the isolator, the return loss of the LNA is not critical for this application. Taking the typical input power of the LNA into account, its input P1dB must be higher than −105 dBm. Although the gain specification of the LNA highly depends on the noise of the following stages, it can typically be set to 40 dB. The LNA specifications required for 6–8 GHz readout operation are summarized in Table I based on the analysis above.

III. Circuit Analysis

The LNA topology is given in Fig. 2. The inverter topology has been chosen to double the transconductance for the same

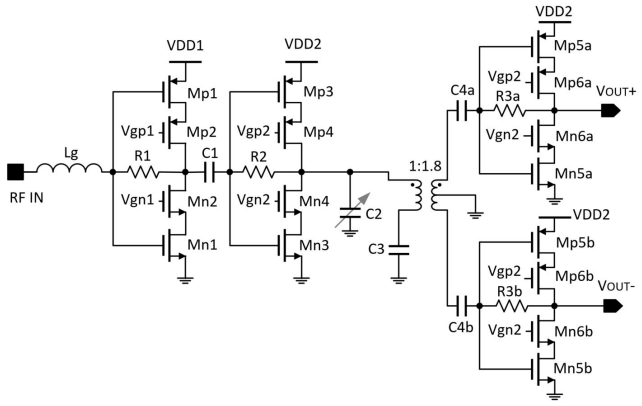

Fig. 2. Schematic of the three-stage cascoded inverter LNA.

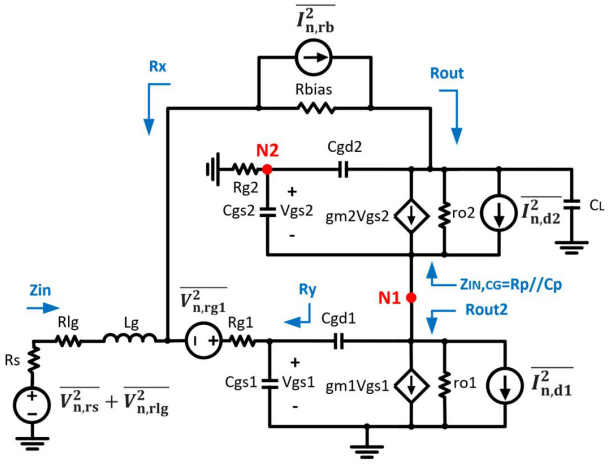

Fig. 3. Small-signal equivalent circuit of the first stage of the cascoded inverter LNA with the gate inductor including main noise sources. C_{ds} of the transistors and the thermal noise of R_{g2} are neglected.

current consumption so that low-power consumption can be achieved for a targeted noise performance [20]. The inverter topology is used in various applications. For example, in [21], an inverter LNA with the complementary transconductance linearization method trades power consumption for high linearity targeting SAW-less receiver applications, and it utilizes the capacitive load to reduce the effect of the gate inductor on the NF. Also, [22] shows that cascode inverter-based TIA can provide very high transimpedance gain at low frequencies, which makes it suitable for high-sensitivity biomedical applications. On the other hand, in quantum computing applications, high linearity performance is not needed, and low power consumption is crucial. Moreover, the noise contribution of lossy passive components becomes less important at low physical temperatures. Therefore, for this particular application, the inverter LNA design is optimized for high gain, low power consumption, and lower noise contribution of the active devices. Cascode transistors are added since they provide a high voltage gain by reducing the required loading capacitor for the input impedance matching as explained in Section III-B. Moreover, the input impedance optimization results in a larger valued gate inductor in the presence of cascode transistors, which provides a higher passive gain.

The input transistors of the cascoded inverter LNA are self-biased by a large resistor between the input and output. The gates of cascode transistors are biased by ON-chip voltage generators, which are programmable resistor DACs via SPI. The LNA comprises three stages of cascoded inverters to have a sufficient gain in order to overcome the baseband noise. The single-ended output of the second stage is transformed into a differential signal via a balun whose resonance frequency is tuned by the variable capacitor, $C2$.

For the analysis of gain, input impedance, and noise, the small-signal equivalent circuit of the first stage with the gate inductor is given in Fig. 3. For the simplicity of the circuit analysis, PMOS and NMOS transistors of the inverter are combined and represented as a single transistor in Fig. 3. Considering that the difference between their small-signal parameters is about 10%, this assumption poses only a small error in the hand calculations. The C_L represents the input capacitance of the second stage. The input parallel resistance of the second stage has typically a very high value; therefore, it is neglected here. In the input impedance and gain analysis, the effect of R_{bias} is also omitted since its value is typically very high.

A. Gain

The total voltage gain of the first stage including the passive gain of the gate inductor can be written as

$$A_V = \frac{V_{\text{gs1}}}{V_{\text{in}}}\frac{V_{\text{out}}}{V_{\text{gs1}}} \tag{2}$$

where the first and second terms are the passive gain of the gate inductor and the voltage gain of the cascoded inverter, respectively. Assuming that $Z_{\text{in}} = R_s$ at the operating frequency, ω_0, the passive gain can be expressed as

$$\left|\frac{V_{\text{gs1}}}{V_{\text{in}}}\right| = \frac{1}{R_s}\sqrt{(R_s - R_{lg} - R_{g1})^2 + \omega_0^2 L_g^2} \approx \frac{\omega_0 L_g}{R_s} \tag{3}$$

where R_s, R_{lg}, and R_{g1} are the input source resistance, the series parasitic resistance of the gate inductor, and the gate resistance of the input transistors, respectively [20]. Equation (3) indicates that the passive gain is proportional to the value of the gate inductor. The gain of the cascoded inverter can be found as

$$\left|\frac{V_{\text{out}}}{V_{\text{gs1}}}\right| \approx \frac{g_{m1}}{\omega_0(C_L + C_{o,\text{inv}})} \tag{4}$$

where

$$C_{o,\text{inv}} \approx C_{\text{gd2}} + (C_{\text{gd1}} + C_{\text{gs2}})/(g_{m2}r_{o2}). \tag{5}$$

In a high-frequency operation, the loading capacitor (C_L) should be small enough to obtain a decent gain. In this case, the total capacitance seen from the output of the inverter ($C_{o,\text{inv}}$) becomes comparable to C_L; therefore, $C_{o,\text{inv}}$ is not neglected here. For instance, $C_L \approx C_{o,\text{inv}}$ for the selected device sizes in Section IV-B.

B. Input Impedance Matching

The input impedance of the common source (CS) transistor M1 is dependent on the load that it experiences from the common gate (CG) transistor M2. The input impedance of the CG (marked as $Z_{\text{in,CG}}$ in Fig. 3) can be expressed as the parallel combination of a resistance (R_p) and a capacitance (C_p) which can be derived as

$$R_p \approx \frac{\alpha+1}{\alpha}\frac{1}{g_{m2}} \tag{6}$$

$$C_p = \frac{g_{m2}r_{o2}C_L}{\alpha+1} + C_{\text{gs2}} \approx \frac{g_{m2}r_{o2}C_L}{\alpha+1} \tag{7}$$

where $\alpha = C_L^2\omega_0^2 r_{o2}^2$. The resulting imaginary and real part of the LNA input impedance can then be expressed based on the small-signal equivalent circuit in Fig. 3 as

$$\text{Im}[Z_{\text{in}}] = \omega_0 L_g - \frac{(C_M + C_{\text{gs1}}) + \omega_0^2 R_{p2}^2 C_T (C_p + C_{\text{gd1}})}{\omega_0\left((C_M + C_{\text{gs1}})^2 + \omega_0^2 R_{p2}^2 C_T^2\right)} \tag{8}$$

$$\text{Re}[Z_{\text{in}}] = R_{lg} + R_{g1} + \frac{R_{p2}C_{\text{gd1}}(C_M + C_p g_{m1} R_{p2})}{(C_M + C_{\text{gs1}})^2 + \omega_0^2 R_{p2}^2 C_T^2} \tag{9}$$

where

$$R_{p2} = R_p // r_{o1} \approx R_p \tag{10}$$

$$C_T = C_p C_{\text{gd1}} + C_p C_{\text{gs1}} + C_{\text{gd1}} C_{\text{gs1}} \approx C_p C_{\text{gs1}} \tag{11}$$

$$C_M = C_{\text{gd1}}(1 + g_{m1} R_{p2}) \tag{12}$$

Equations (10) and (12) show that the Miller capacitor, C_M, becomes smaller in the presence of the cascode transistor due to its small input impedance (R_p). Hence, because of the reduced Miller effect, $C_M < C_{\text{gs1}}$ can be assumed for cascoded inverters. Also, by assuming $C_{\text{gd1}} \ll C_{\text{gs1}}$, and considering approximations in (7), (10), and (11), (8) and (9) can be simplified as follows:

$$\text{Im}[Z_{\text{in}}] \approx \omega_0 L_g - \frac{1}{\omega_0 C_{\text{gs1}}} \tag{13}$$

$$\text{Re}[Z_{\text{in}}] \approx R_{lg} + R_{g1} + \frac{g_{m1}C_{\text{gd1}}}{g_{m2}r_{o2}C_L\omega_0^2 C_{\text{gs1}}^2}. \tag{14}$$

With lowered C_M, the imaginary part of the cascoded inverter's input impedance is reduced and dominated by C_{gs1} as shown in (13). This allows us to employ a larger L_g for the input impedance matching and thus obtain a higher passive gain.

The last term in (9) indicates that $\text{Re}[Z_{\text{in}}]$ has a positive value when there is a capacitive loading at the output of the first stage. This eliminates the need for a source degeneration inductor to obtain positive real input impedance. Also, $\text{Re}[Z_{\text{in}}]$ is created through the capacitive feedback of C_{gd1}, and the real input impedance of the cascoded inverter becomes zero when C_{gd1} is zero. If we compare $\text{Re}[Z_{\text{in}}]$ in (14) with the real input impedance of an inverter without cascode in (15) [20], it can be clearly seen that C_L is multiplied by the intrinsic gain of the cascode transistor

$$\text{Re}[Z_{\text{in},w/o\text{casc}}] \approx R_{lg} + R_{g1} + \frac{g_{m1}C_{\text{gd1}}}{C_L\omega_0^2 C_{\text{gs1}}^2}. \tag{15}$$

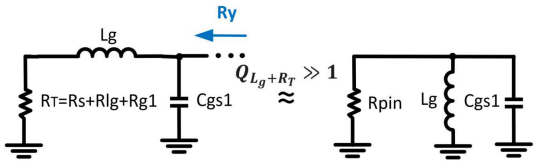

Fig. 4. Simplified equivalent circuit for R_y.

For inverters without cascode, C_L needs to be in the pF range, or g_m should be much smaller to obtain 50 Ω input impedance. Both ways lead to a very low voltage gain considering that the inverter gain is inversely proportional to C_L, and it is commensurate with g_m as shown in (4). Assuming that $g_m r_o$ is around 10 V/V for short-channel devices, this reduces the required C_L value for the input impedance below 200 fF as shown in Section IV-B, which is a more practical value to be realized by the second stage.

C. Noise Analysis

The main noise sources of the LNA are R_{lg}, R_{g1}, R_{bias}, and the channel thermal noise of the transistors as illustrated in Fig. 3. The output-referred noise of the channel thermal noises can be expressed as

$$\overline{V_{n,d1,o}^2} = \overline{I_{n,d1}^2}|R_{N1}|^2|A_{1,o}|^2 \tag{16}$$

$$\overline{V_{n,d2,o}^2} = \frac{\overline{I_{n,d2}^2}}{g_{m2}^2}|A_{2,o}|^2 \tag{17}$$

where $\overline{I_{n,d1}^2} = 4kT\gamma g_{m1}$ and $\overline{I_{n,d2}^2} = 4kT\gamma g_{m2}$. $A_{1,o}$ and $A_{2,o}$ are the gain from N1 and N2 to the output of the first stage, respectively. R_{N1} given below is the total impedance seen from node N1.

$$R_{N1} = R_{\text{out2}} // Z_{\text{in,CG}} \approx R_{\text{out2}} // C_p \tag{18}$$

where R_{out2} is the output impedance of the CS transistor. The magnitude of $Z_{\text{in,CG}}$ is typically dominated by C_p; thus, R_p can be neglected.

To ease the calculation of R_y, the input side of the LNA can be rearranged as shown in Fig. 4 by assuming that the Q-factor ($\omega_0 L_g/(R_s + R_{g1} + R_{\text{lg}}) > 1$) is higher than unity

$$R_{\text{pin}} \approx Q_{(L_g+R_T)}^2 R_T \approx \frac{\omega_0^2 L_g^2}{R_s + R_{lg} + R_{g1}} \approx \frac{\omega_0^2 L_g^2}{R_s}. \tag{19}$$

Assuming that L_g resonates with C_{gs1}, $R_y \approx R_{\text{pin}}$. By neglecting $1/r_{o1}$ and considering that $\omega_0 C_{\text{gd1}} R_y \ll 1$, R_{out2}, $A_{1,o}$, and $A_{2,o}$ can be found as

$$R_{\text{out2}} = \frac{1 + j\omega_0 C_{\text{gd1}} R_y}{j\omega_0 C_{\text{gd1}}(1 + g_{m1}R_y)} \approx \frac{R_s}{j\omega_0^3 C_{\text{gd1}} g_{m1} L_g^2} \tag{20}$$

$$A_{1,o} \approx \frac{g_{m2}}{j\omega_0(C_L + C_{\text{gd2}}) + 1/r_{o2}} \tag{21}$$

$$A_{2,o} \approx \frac{g_{m2}}{(1 + g_{m2}R_{\text{out2}})}\frac{R'_{\text{out}}}{j\omega_0(C_L + C_{\text{gd2}})R'_{\text{out}} + 1} \tag{22}$$

where $R'_{\text{out}} = g_{m2}r_{o2}R_{\text{out2}} + r_{o2} + R_{\text{out2}}$. The output-referred noise of the R_{bias} can be derived as

$$\overline{V_{n,rb,o}^2} = \overline{I_{n,rb}^2}|R_x A_{1,o} + R_{\text{out}}|^2 \tag{23}$$

where $R_x = (R_s - j\omega_0 L_g)//(R_s + j\omega_0 L_g)$ when the input impedance is matched. Then, $R_x \approx \omega_0^2 L_g^2/(2R_s)$ assuming that $\omega_0 L_g \gg R_s$. So, the input-referred noise of R_{bias} is

$$\overline{V_{n,rb,i}^2} \approx \frac{4kT}{R_{\text{bias}}}\omega_0^2 L_g^2. \tag{24}$$

Equation (24) indicates that the input-referred noise of R_{bias} increases with the operating frequency and the gate inductor value. After dividing the output-referred noises by the total gain and omitting the noise of the second and third stages, the NF of the cascoded inverter LNA can be written as

$$F = 1 + \frac{R_{lg}T_a}{R_s T_0} + \frac{4R_{g1}R_s T_a}{\omega_0^2 L_g^2 T_0} + \frac{\omega_0^2 L_g^2 T_a}{R_{\text{bias}} R_s T_0} + \frac{4\gamma\, g_{m1}\left|A_{1,o}\right|^2 |R_{N1}|^2 T_a}{R_s |A_v|^2 T_0} + \frac{4\gamma\left|A_{2,o}\right|^2 T_a}{R_s g_{m2} |A_v|^2 T_0} \tag{25}$$

where T_0 (typically 290 K) and T_a are the reference and ambient temperatures, respectively. At RT, the thermal noise of the gate inductor is typically the dominant noise source of the LNA because of the low Q-factor of ON-chip inductors and the suppression of the other noise sources by the passive gain of the gate inductor. The channel noise of the input and cascode transistors (the fifth and sixth terms in (25), respectively) contributes the most to the overall NF after the thermal noise of the gate inductor. According to (25), the input-referred noise of $\overline{I_{n,d1}^2}$ and $\overline{I_{n,d2}^2}$ becomes lower with a higher g_{m1}. On the other hand, increasing g_{m2} raises the input-referred noise of $\overline{I_{n,d1}^2}$ while it slightly reduces the input-referred noise of $\overline{I_{n,d2}^2}$. As a result, a lower g_{m2} provides less NF in total considering that the input-referred noise of $\overline{I_{n,d1}^2}$ is more significant than of $\overline{I_{n,d2}^2}$. Therefore, a high g_{m1} and low g_{m2} are required at the same time for optimum NF performance, which can be achieved by employing smaller cascode transistors compared to input transistors. This also reduces the total load capacitance thereby providing a higher A_v. Additionally, according to (20), R_{out2} is inversely proportional to L_g^2. Therefore, increasing L_g lowers the input-referred noise of $\overline{I_{n,d1}^2}$ and raises the input-referred noise of $\overline{I_{n,d2}^2}$ as also illustrated in Section IV-B. The thermal noise of R_{bias} and R_{g1} is usually the least critical noise source since they can be made negligible by increasing the value of R_{bias} and transistor finger number.

IV. Low-Power Cryogenic LNA Design

Even though cryogenic circuit design is now an active field, especially in quantum computing applications, there is still no available compact CMOS model covering the dc and RF characteristics of MOSFETs at deep cryogenic temperatures. Thus, we designed the LNA using standard RT models provided by the foundry and the circuit analysis presented in Section III. Also, variations on inductors and the small-signal parameters of transistors from RT to 4 K reported in the literature are considered during the LNA design.

A. Design Considerations for 4 K Operation

As well known, the threshold voltage of transistors increases due to incomplete ionization at low temperatures. For 28 nm NMOS and PMOS devices, $\triangle V_T$ is around 0.12 and 0.2 V at 4 K, respectively, and it slightly changes with the device size [23]. Since V_{DD} is shared with V_{gs} of two transistors in the self-biased inverter topology, ultra-low V_T devices are employed to avoid operating CS transistors in the subthreshold region at 4 K. By the same token, the LNA design at RT is done with 0.8 V V_{DD} to give some margin for the V_T shift at 4 K.

The reduction in phonon scattering raises the mobility of NMOS and PMOS transistors by three times, and this increases the g_m of the transistors ~30% at 4 K in the 28 nm technology node [23]. As given in (13) and (14), the shift on g_m of CS and CG transistors cancels each other in the real part of the input impedance, and the imaginary part does not depend on g_m. Thus, we expect that the input impedance of the LNA has a low sensitivity to g_m. Also, g_{ds} stays almost the same between 4 K and RT [23], [24]. Therefore, we anticipate that the gain will increase 30% in each stage, 6.8 dB in total due to the higher g_m at 4 K. In [24], it is reported that C_{gs} changes a negligible 1% from 293 to 6 K for a 32 nm SOI CMOS transistor at the same current density while C_{gd} does not change by temperature.

Measurements on test structures have shown that the sheet resistance of top metals in the 28 nm CMOS process decreases by a factor of 20 from 300 to 4 K. Also, the substrate loss becomes negligible because of its high resistive nature induced by the carrier freeze-out. These substantially improve the Q-factor of inductors [25]. On the other hand, the lower sheet resistance of metals at 4 K reduces the skin depth and inductance values (~5%) of inductors. Hence, the skin effect becomes more dominant for the Q-factor of inductors at 4 K. The significant reduction on the series resistance of inductors will result in a much lower R_{lg} in (9) meaning a lower real input impedance at 4 K.

Although due to its dependency on C_{gs}, C_{gd}, and g_{ds}, the LNA input matching can shift by up to ~400 MHz with process variations according to simulation results, g_m has an insignificant effect on the input impedance, and C_{gs}, C_{gd}, and g_{ds} vary negligibly by the temperature at the same current density as discussed above. Thus, we do not expect a significant change in the input impedance of the cascoded inverter at the same current consumption from RT to 4 K. The main variation in the total input impedance will occur due to the lower series resistance and inductance of the gate inductor at 4 K. However, this can be tolerable considering that the real input impedance is created largely by the cascoded inverter, and the frequency shift of the impedance matching due to the inductance change will be around 200 MHz for the 6–8 GHz bandwidth. Therefore, the input impedance matching has been done according to RT simulations.

Thermal noise is the dominant noise source for RT LNAs in high-frequency operations. Therefore, as demonstrated in [26] and [27], the noise temperature of CMOS LNAs improves proportionally to the ambient temperature (down to 77 K). However, some cryo-CMOS LNAs at 4 K in [2] and [13] show that in spite of a 75 times reduction in the physical temperature, this improvement is only 6–8 times, which is even less (three times) in [8]. This is attributed to self-heating

and shot noise so far in the literature. In [12], it is shown that the gate temperature of transistors stays almost the same below 20 K for given power consumption in the channel, and the local self-heating can reach 55 K with 6 mW power consumption at 4 K. Thus, the power dissipation in the first stage should be kept low to avoid significant thermal noise.

According to noise characterizations of nanoscale MOSFETs in [11], shot noise becomes more prominent in the strong inversion region of the short channel devices and becomes dominant for 10 nm MOSFETs. This is due to the fact that in short channel devices, the mean free path of carriers is higher than the effective channel length, and some carriers travel across the channel without incurring any scattering event. This quasi-ballistic transport of carriers causes fluctuation in the drain current due to the discrete nature of the carriers thereby forming shot-like noise in the channel [9]. Taking the phonon scattering reduction into account, the shot noise might be even more severe at 4 K, however, there are no experimental results provided in the literature regarding the shot noise at cryogenic temperatures. At RT, the drain current noise model including shot noise is modeled as

$$\overline{I_{n,d}^2} = 4kT\gamma\, g_m(1-F) + 2q\sigma\, I_D F \tag{26}$$

where F, σ, and q are shot noise suppression, shot noise excess noise factor, and elementary electron charge, respectively [28]. According to RT measurements, the shot noise is suppressed by a longer channel length and higher $V_{\rm gs}$ [9], [11]. Increasing the channel length also raises the threshold voltage, and $V_{\rm gs}$ of the PMOS and NMOS input transistors in the cascoded inverter LNA are limited by $V_{\rm DD}$. Based on these factors, the channel length of all transistors is chosen as 50 nm instead of the minimum channel length. In 28 nm CMOS technology, the shot noise suppression factor for 50 nm channel length is around 0.45 when $V_{\rm gs} = 0.6$ V and $V_{\rm ds} = 0.4$ V, and it slightly differs for NMOS and PMOS devices [29].

There is no static power consumption on the gate inductor, and the self-heating becomes quite small at the distance of 1 μm away from the heat source at 4 K [12]. Moreover, $R_{\rm lg}$ is highly reduced at 4 K; therefore, its thermal noise will be very small. Also, the power dissipation on $R_{\rm bias}$ is practically zero thereby inducing a little thermal noise contribution. Even though the gate resistance, R_{g1}, is severely affected by the self-heating of the transistor, the gate resistance can be minimized by increasing the transistor finger number as much as possible to significantly reduce its thermal noise.

Based on the above discussion, we believe that the channel noise is the dominant noise source due to the shot noise and self-heating at 4 K. By assuming that the shot noise portion of the channel noise in (26) is the same at 4 K as at RT, the NF and power dissipation of the cascoded inverter LNA are optimized by taking only the channel noise of the transistors into account.

B. LNA Implementation

First, $V_{\rm DD}$ and the channel length of transistors are thus chosen to 0.8 V and 50 nm, respectively, considering the device operations at cryogenic temperatures as explained in Section IV-A. For each transistor, the finger width is set to 500 nm to minimize the gate resistance. Also, $R_{\rm bias}$ is chosen as 13 kΩ to make it a practically open circuit for ac.

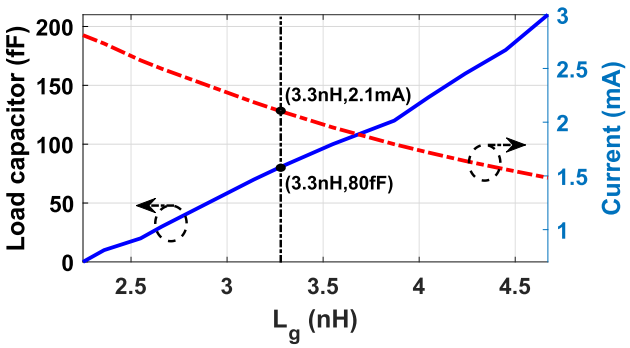

Fig. 5. Value of L_g versus the current consumption and loading capacitor of the first stage (C_L) according to simulations that achieves $Z_{\rm in} = 50 + j.0\ \Omega$.

Second, the gate inductor (L_g) of the first stage is swept to find the optimum point for the total channel noise and power consumption. For each L_g value, there is only a single value of C_L and the transistor width (initially same for all transistors) to obtain 50 Ω input impedance. Fig. 5 shows the values of resultant C_L and current consumption after the input impedance matching is adjusted by specter simulations for each L_g value. For each design point in Fig. 5, the input-referred noise temperatures of the channel noises and the total gain in the first stage with the load capacitor are given in Fig. 6. As consistent with the theory in Section III-C, a higher L_g induces more $T_{n,d2}$ and less $T_{n,d1}$. Even though a higher L_g requires a smaller input transistor as well as a lower g_m for the input impedance matching, the sum of input-referred noise of channel currents stays almost the same thanks to the higher passive gain of L_g. This allows us to select an operating point with a lower power consumption without having any penalty for the noise performance of the first stage. The main constraint here is the gain of the first stage which degrades with a higher load capacitor and lower g_m. Considering that the first stage should have a sufficiently high gain in order to suppress the noise of the rest, we aimed to achieve a minimum 20 dB gain in the first stage; thus, we chose the design point with $L_g = 3.3$ nH and $C_L = 80$ fF where the current consumption is 2.1 mA. The load capacitance of 80 fF corresponds to approximately half the size and transconductance of the first stage, and hence the current consumption of 1 mA. Despite the lower g_m, the noise contribution of the second stage is still negligible owing to the high gain in the first stage. Thus, it is convenient to be realized by the second stage in terms of noise and power dissipation.

Noise contributions of the gate inductor, $R_{\rm bias}$, and the gate resistance (R_{g1}) at RT are shown in Fig. 7. The input-referred noise of $R_{\rm bias}$ increases with a larger L_g as also given in (24). The input-referred noise of the gate inductor is the main noise source at RT due to its high parasitic series resistance. However, we expect that the thermal noises of $R_{\rm lg}$, $R_{\rm bias}$, and R_{g1} will be negligible at 4 K.

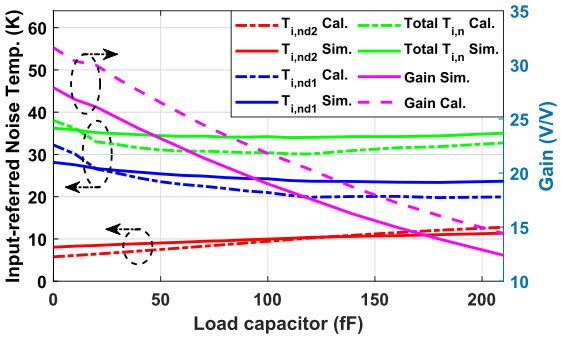

Fig. 6. Calculated and simulated input-referred noise temperatures of CS ($T_{i,nd1}$) and CG ($T_{i,nd2}$) transistors and the total gain of the first stage (including the passive gain) versus C_L. The calculations are done using the circuit theory provided in Section III.

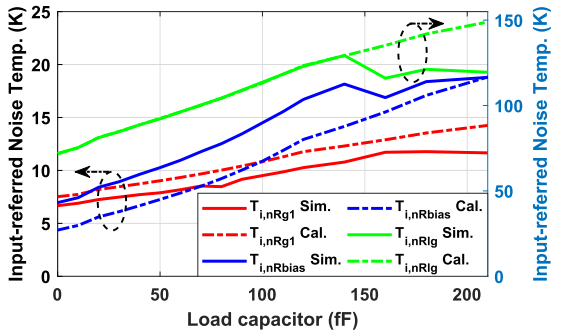

Fig. 7. Calculated and simulated input-referred noise temperatures of R_{lg}, R_{bias}, and R_{g1} versus C_L. The calculations are done using the circuit theory provided in Section III.

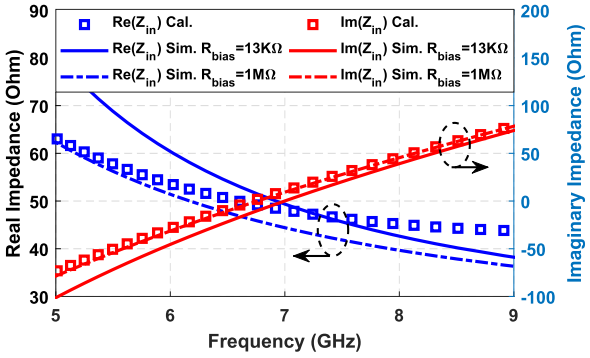

Fig. 8. Simulated and calculated input impedances at RT.

For the selected device sizes and operating point, the calculated and simulated input impedances of the LNA are plotted in Fig. 8. It indicates that the feedback effect of the biasing resistor of 13 kΩ, which is neglected in (8) and (9), shifts the input impedance only 10% between 6–8 GHz bandwidth thereby causing a slight deviation between hand calculation and simulation. In Fig. 9, it is shown that even if we double the g_m of all transistors, there is only a negligible variation in the input impedance. Therefore, the difference of g_m between 4 K and RT is not a concern for impedance matching. On the other hand, Re[Z_{in}] is reduced by 30% due to the higher Q-factor

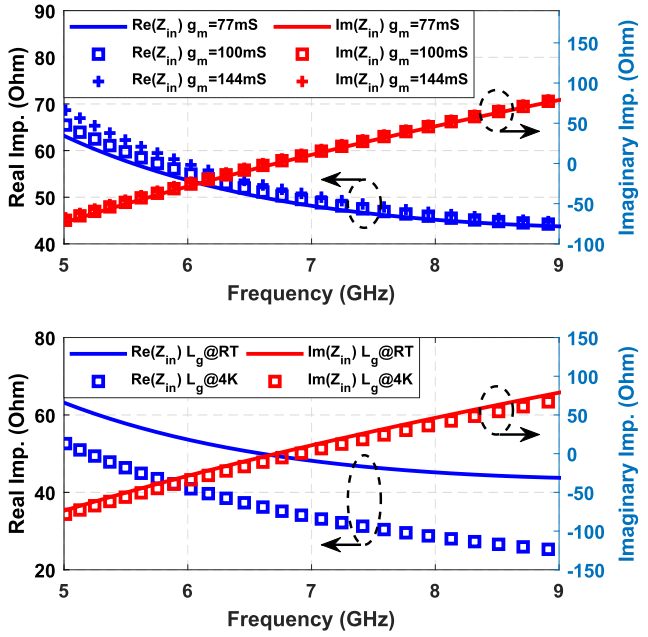

Fig. 9. Dependence of Re[Z_{in}] and Im[Z_{in}] on L_g (bottom) and g_m (top) at 4 K and RT.

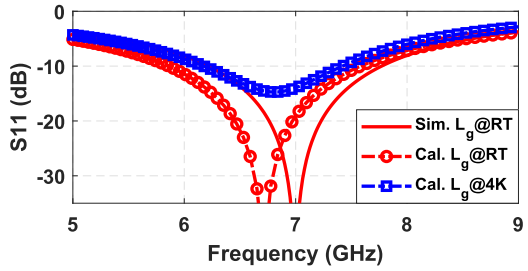

Fig. 10. Dependence of S_{11} on L_g at 4 K and RT by assuming that its Q-factor is five times higher, and its inductance is 5% lower at 4 K.

of the gate inductor at 4 K. Even so, S_{11} at 4 K is less than −10 dB between 6.2 and 7.4 GHz (Fig. 10).

Subsequently, the size of the CG transistors is halved to optimize the NF by reducing the transconductance of CG transistors as explained in Section III-C. After the implementation of the first stage, transistors in the second stage are sized such that they will provide the right amount for the capacitive loading (C_L) as selected in the previous step.

Next, a narrow-band transformer and 5-bit tunable capacitor covering 6–8 GHz bandwidth are implemented together with the third stage to provide a differential output. At last, ESD diodes are added for each pad including the RF input, and the values of the circuit elements and transistor sizes are slightly re-optimized after parasitic extraction in the whole circuit and EM simulation of inductors together with the input pad. Also, a part of the gate inductor is realized by a bondwire of 0.75 nH. The EM simulation of the gate inductor at 4 K is performed using the measured sheet resistance of the top metals and by setting substrate conductivity to zero. According to the EM simulation, DC ohmic loss and skin effect almost equally contributes to the total loss on the gate inductor at 8 GHz at RT. Since the skin depth is proportional to the square root

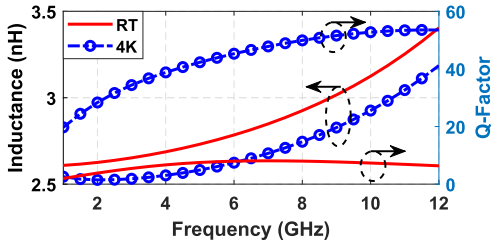

Fig. 11. EM simulation of the gate inductor at 4 K and RT.

TABLE II
LNA CIRCUIT PARAMETERS

Components	Values	Transistors	Dimensions
L_g	2.85 nH	Mn1 and Mp1	52 μm
R1,2,3a,3b	13 KΩ	Mn2 and Mp2	26 μm
C1	515 fF	Mn3 and Mp3	26 μm
C2	490-1480 fF	Mn4 and Mp4	13 μm
C3	1.36 pF	Mn5a,b and Mp5a,b	28 μm
C4a,b	1.52 pF	Mn6a,b and Mp6a,b	14 μm
L2p, L2s	260 pH, 870 pH		

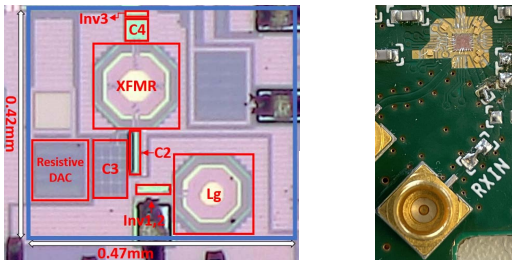

Fig. 12. Chip micrograph of the 28 nm CMOS LNA (left) and the readout die wirebonded on a test PCB (right).

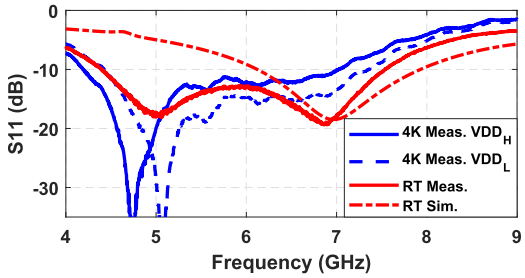

Fig. 13. Measured S_{11} at 4 K and RT.

of the copper resistivity [25], the loss due to the skin effect is reduced by $\sqrt{20}$ times at 4 K. Therefore, despite a 20× improvement of the top metal conductivity, the Q-factor of the gate inductor increases by only six times and goes up to 50 at 8 GHz; moreover, its inductance is 5% less at 4 K as shown in Fig. 11. The final values of the devices and transistor sizes are given in Table II.

V. MEASUREMENT RESULTS

The designed LNA has been fabricated as part of a readout SoC in a 28 nm bulk CMOS process, and its die is wire-bonded

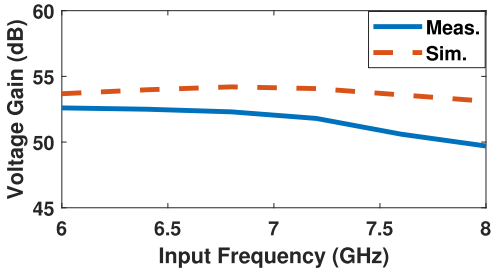

Fig. 14. Simulated and measured gain of the LNA at RT, where C_2 is tuned for each frequency point to obtain the highest gain.

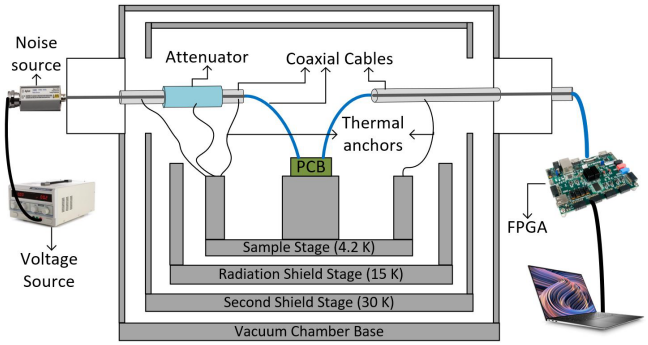

Fig. 15. Diagram of 4 K noise measurement setup.

on the test PCB as shown in Fig. 12. The LNA size is approximately 0.2 mm^2 excluding pads. The RF input line on the PCB is a coplanar waveguide with the ground providing 50 Ω characteristic impedance, and it does not include any discrete component employed for the input impedance matching or AC coupling capacitor. For cryogenic measurements, the test PCB was inserted into the 4 K stage of a cryogenic probe station in a vacuum condition. Since small-signal parameters of MOSFETs affecting the input impedance of the cascoded inverter LNA stays almost the same at 4 K with the same current density as at RT as explained in Section IV-A, we have performed the characterization of the LNA at RT and 4 K with 0.86 and 1.04 V (V_{DD_H}), respectively, which provide the same current consumption (4.1 mA) at both temperatures. According to the RT CMOS model, V_{gs} values of CS transistors are close to their V_{th} for the selected V_{DD} at RT. This facilitates keeping each transistor in the saturation region by minimizing V_{dsat}. Considering the higher V_{DD}, there is even more headroom for each transistor at 4 K. The gate voltages of cascode transistors were experimentally adjusted to operate transistors in the saturation region at 4 K and RT. $V_{gp1,2}$ and $V_{gn1,2}$ are set to 135 mV (120 mV) and 620 mV (700 mV) at RT (4 K), respectively. Moreover, the LNA has been measured with a lower supply voltage ($V_{\mathrm{DD}_L} = 1$ V) at 4 K to investigate its noise performance at a lower power consumption (2.5 mW). At RT, Fig. 13 shows that there is one additional notch around 5 GHz in the measured S_{11}, and the input impedance matching is shifted toward lower frequencies in the measurement results compared to simulations. The differences may stem from the input line on the PCB, which is not characterized at RT and not included in the simulations. S_{11} is lower than −10 dB

TABLE III
PERFORMANCE COMPARISON OF THE DESIGNED CRYOGENIC LNA WITH PRIOR WORKS

Ref.	Topology	Frequency (GHz)	Temperature	NF (dB)	Power (mW)	Gain (dB)	S11 (dB)	Area (mm^2)	Technology
[2]	Noise cancelling	0.1-0.5	300 K	0.8-1.25	80	35-40	<-5	0.249[1]	160 nm CMOS
			4.2 K	0.1-0.85	91	50-58	<-3		
[8]	Cascoded CS + inductive degeneration + gate L	4.1-7.9	300 K	0.75-1.3	51.1	35.5-36.5	<-12	0.72	40 nm CMOS
		4.6-8.2	4.2 K	0.23-0.65	39	39.2-44.8	<-5.8		
[13]	Cascoded CS + inductive degeneration	6-8	300 K	2.5[4]	70[2]	-	-	-	40 nm CMOS
			4.2 K	0.6[4]	66[2]	-	-		
[27]	Cascoded CS + inductive degeneration + gate L	2.02-2.12	300 K	1.56-1.93	15.4	15.5	<-12	0.49	180 nm CMOS
			77 K	0.5	15	18	<-15		
This work	Cascoded inverter + C-feedback + gate L	6-8	300 K	2.5-3.5	3.5	54[3]	<-6	0.2[1]	28 nm CMOS
			4.2 K	0.4-0.7	4.2	-	<-4		

[1]Excluding the pads, [2]Power consumption of the whole receiver, [3]Simulated gain, [4]NF of the whole receiver.

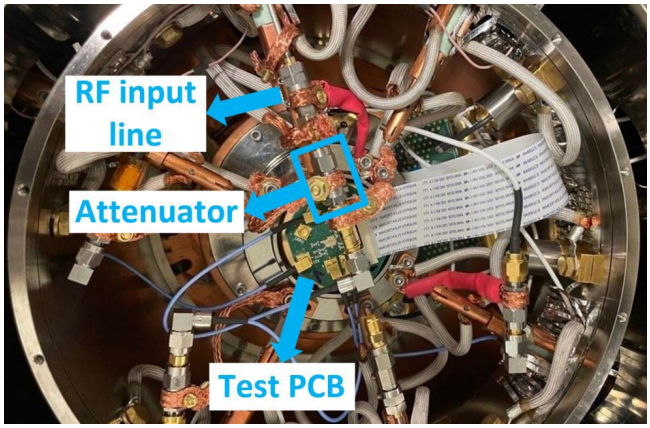

Fig. 16. 4 K noise measurement setup in the cryo-probe station including the cryo-attenuator.

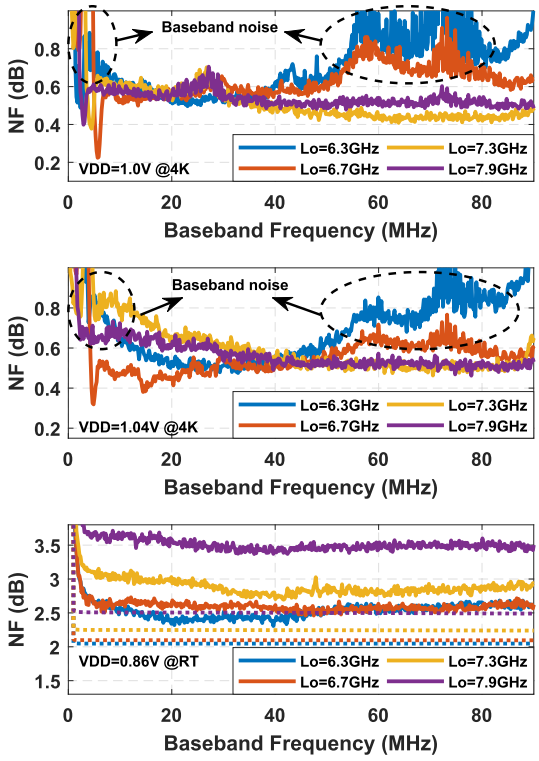

Fig. 17. Measured NF at 4 K and RT (solid lines) and simulated NF at RT (dotted lines).

between 4.2–7.2 GHz (4.4–7.5 GHz) at 4 K (300 K) when $V_{\mathrm{DD}} = V_{\mathrm{DD}_H}$. With V_{DD_L}, the input impedance matching is slightly shifted to higher frequencies.

Since we cannot measure the LNA gain individually, the approximate gain of the LNA at RT is extracted by subtracting the simulated baseband gain from the measured gain of the whole receiver as given in Fig. 14. By tuning C_2, the gain of over 50 dB is obtained between 6–8 GHz at RT.

At both 4 K and RT, the Y-factor method was used for NF measurements; moreover, we utilized a 20 dB cryo-attenuator to lower the NF measurement uncertainties at 4 K as proposed in [30]. The cryo-attenuator was placed between the RF input of the LNA and a noise source standing at RT, and the RF input line and the attenuator were thermalized by some copper braids connected to the 4 K stage inside the probe station to ensure that the physical temperature of the attenuator becomes 4 K as shown in Figs. 15 and 16. Since the LNA does not have a separate output for testing purposes, the NF has been measured using the downconverted signals obtained with different local oscillator (LO) frequencies at the outputs of the ADCs. These sampled baseband signals have been fetched by FPGA via a high-speed serial interface, and the NF has been calculated off-chip by post-processing them. Considering the high gain of the LNA shown in Fig. 14, we anticipate that the rest of the receiver chain has a negligible effect on the measured NF, and the measured NF is approximately equal to the NF of the LNA when the LNA operates linearly.

At RT, the NF is between 2.5–3.5 dB as shown in Fig. 17. There is a strong interference of a 200 MHz clock (used for the data conversion in the readout chip) with LNA at both 4 K and RT. Despite the interference, the LNA still behaves linearly at

RT. However, due to the higher gain of the LNA at 4 K, this interference causes the gain compression of the LNA between 6–6.7 GHz. Therefore, the NF is dominated by baseband noise in some parts of the baseband spectrum when LO frequency is 6.3 and 6.7 GHz at 4 K, which is more severe with V_{DD_L} due to the lower gain of the LNA. However, the NF varies between 0.4 and 0.7 dB at the rest of the spectrum. Even though the power consumption is 40% less with V_{DD_L} meaning a lower V_{gs} and V_{ds} for each transistor, the NF negligibly changes in the frequencies where the baseband noise is not prominent. This can be attributed to the fact that the shot noise suppression factor decreases with lower V_{ds} although it is higher with lower V_{gs}. Moreover, reducing power consumption causes less self-heating.

Table III shows the performance comparison of the proposed LNA with other cryo-CMOS LNAs. The designed cascoded inverter-based LNA has a comparable NF performance between 6–8 GHz to the state-of-the-art, and this is achieved with a ten times lower power consumption compared to cascode CS LNAs with a source degeneration inductor.

VI. Conclusion

In this article, an LNA with cascoded inverter topology and a high-Q ON-chip gate inductor is proposed for qubit readout at 4 K. The current consumption for given transconductance is halved using inverter topology. The capacitive feedback is used for realizing the real input impedance matching. To improve the gain, the load capacitor value of the first stage required for the input impedance matching is reduced using cascode transistors. Also, thanks to the reduced Miller capacitance with cascode transistors, a larger gate inductor is employed for the input impedance matching thereby boosting the passive gain. We showed that a similar S_{11} at 4 K and RT can be achieved with cascoded inverter-based LNAs, which eases the circuit design for cryogenic temperatures. Moreover, with the detailed noise analysis of the LNA, we demonstrated that power consumption can be significantly reduced for a given NF by exploiting the high passive gain of a large high-Q gate inductor at 4 K. This makes cascoded inverter topology with a high-Q gate inductor attractive for scalable qubit readout electronics. The LNA achieves 0.4–0.7 dB NF and over 50 dB gain between 6–8 GHz with 4.2 mW power consumption (0.042 mW/qubit), which meets the required LNA specifications for superconducting qubit readout applications.

Acknowledgment

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